# **EAST Search History**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1038	703/14.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/08/06 17:02
L2	78	703/14.ccls. and @pd>"20060401"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/08/06 17:08
L3	8	09/724,585	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/08/06 17:43
L4	1953	instrumentation and statistic\$1 and @ad<"20010901"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/08/06 17:44
L5	665	L4 and (logic or hdl or verilog or vhdl)	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/08/06 17:45
, L6	300	L5 and (simulat\$4 or emulat\$4)	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/08/06 17:45

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Results 1 - 10 of about 6,700 for instrumentation logic simulation. (0.15 seconds)

#### Fault modeling and logic simulation of CMOS and MOS integrated circuits group of 2 »

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RL Wadsack - Bell System Technical Journal, 1978 - adsabs.harvard.edu

Title: Fault modeling and logic simulation of CMOS and MOS integrated circuits Authors:

Wadsack, R. L. Journal: Bell System Technical Journal, vol. ...

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#### HITEC: a test generation package for sequential circuits - group of 2 »

T Niermann, JH Patel, STS Inc, CA Los Altos - Design Automation. EDAC. Proceedings of the European ..., 1991 ieeexplore.ieee.org

... circuits, Iyengar, V.; Chakrabarty, K.; Murray, BT Instrumentation and Measurement ...

48, Efficient sequential test generation based on logic simulation, Shuo Sheng ...

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## Dynamic test emulation for EDA-based mixed-signal test developmentautomation - group of 2 »

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... Modeling of the ATE instrument, the DUT and the ... on a solution [8], A mixed-signal

simulation backplane simulates ... switch-level, gate-level logic, and behavioral ...

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#### Testing conventional logic and memory clusters using boundary scandevices as virtual ATE channels

P Hansen, T Inc, MA Boston - Test Conference, 1989. Proceedings. Meeting the Tests of ..., 1989 - ieeexplore.ieee.org ... and while a few commercial devices such as Texas Instruments' SCOPETM OCTAL ... which are applied against the cluster model in logic and fault simulation. ...

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#### <u>Virtual Test of Noise and Jitter Parameters - group of 4 »</u>

K Helmreich, G Reinwardt - Proc. International TestConference, 1996 - doi.ieeecomputersociety.org ... and tester components even for virtual logic test. ... tester modelling to modelling the various instruments as individual ... and to rely on the simulation clock to ...

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CR Rupp, M Landguth, T Garverick, E Gomersall, H ... - FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE ..., 1998 - ieeexplore.ieee.org

... with inadequate debugging and instrumentation support ... typically initiate direct

configurable logic pipeline action ... development, run time support, and simulation ....

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#### <u>Unifying simulation and execution in a design environment for FPGA systems - group of 4 »</u>

BL Hutchings, BE Nelson - Very Large Scale Integration (VLSI) Systems, IEEE ..., 2001 - ieeexplore ieee.org

... To illustrate the use of instrumentation code in both simulation and execution a

complete but ... public class traffic extends Logic implements Observable f ...

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# Functional design verification by multi-level simulation - group of 2 »

K Tham, R Willoner, D Wimp - Proceedings of the 21st conference on Design automation, 1984 - portal acm.org

... A simulator, #SIM, acts as an instrumentation shell around the MAINSAIL model allowing ...



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<u>Applied Superconductivity, IEEE Transactions on</u>
Volume 11, Issue 4, Dec. 2001 Page(s):4200 - 4303

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## Tri-state bus conflict checking method for ATPG using BDD - group of 3 »

All articles Recent articles

Y Koseko, T Ogihara, S Murai - Proceedings of the 1993 IEEE/ACM international conference on ..., 1993 - portal.acm.org

... Table 1 **Statistics** of busses and sclcclors #of Outputsof ... are detected that violate the **bus** design rule ... enabling/disabling logic to the **tri- state** drivers for ... Cited by 3 - Web Search - BL Direct

#### <u>Low-power encodings for global communication in CMOS VLSI - group of 6 »</u>

MR Stan, WP Burleson - Very Large Scale Integration (VLSI) Systems, IEEE ..., 1997 - ieeexplore.ieee.org ... for Low Power Until now we have only considered **tri-state** buses on ... decrease in average power dissipation depends on the **statistics** of the **bus** transfers and ... Cited by 83 - Web Search - BL Direct

## <u>DEFUSE</u>: a deterministic functional self-test methodology for processors - group of 11 »

L Chen, S Dey - VLSI Test Symposium, 2000. Proceedings. 18th IEEE, 2000 - ieeexplore.ieee.org ... As Table 2. **Statistics** on the self-test programs ... d1 d2 s1 s2 **bus** d1 d2 s1 s2 **bus tri-state** buffer selector Figure 10. Converting **tri-state** buffers to selectors ... Cited by 40 - Web Search

# A hybrid prototyping platform for dynamically reconfigurable designs - group of 3 »

T Rissa, J Niittylahti - Proc. 10th Int. Workshop on Field-Programmable Logic and ..., 2000 - Springer ... bus is divided in two sections with tri-state drivers. ... to carry out vec- tor multiplications without using any bus resources ... Table 1 . Board physical statistics ... Cited by 3 - Web Search - BL Direct

#### A method to derive application specific embedded processing cores - group of 8 »

O Hebert, IC Kraljic, Y Savaria - Proc. of the 8th Int'l Symp. on Hardware/Software Codesign, 2000 - doi.ieeecomputersociety.org ... The **statistics** described earlier can lead to a number of ... a MAC unit to the destination **bus** of the ... conditions, one of which being a **tri-state bus** driver always ... Cited by 6 - Web Search

#### Time frame generator for X-ray detectors and data acquisition systems for synchrotron radiation ...

JB Khazaie, C Boulin - Nuclear Science, IEEE Transactions on, 1996 - ieeexplore.ieee.org ... several times and accumulate the results to get enough **statistics**. ... Proper isolation of the two **bus** structures using **tri-state** buffers allows the ... Cited by 1 - Web Search - BL Direct

#### MBA. December 1980

S CLEARANCES - 1998 - bus.umich.edu
... Age in Pension Plans," presented at the Bureau of Labor Statistics, Oct. ... Investment
Advice," presented to the annual meeting of the Tri-State Academy of ...
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T Hara, H Ando, C Nakanishi, M Nakaya - Proceedings of the 23rd annual international symposium on ..., 1996 - portal.acm.org Page 1. Performance Comparison of ILP Machines with Cycle Time Evaluation Tetsuya Hara, Hideki Ando, Chikako Nakanishi, Masao Nakaya ...

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#### Modeling design constraints and biasing in simulation using BDDs - group of 3 »

J Yuan, K Shultz, C Pixley, H Miller, A Aziz - Proceedings of the 1999 IEEE/ACM international conference on ..., 1999 - portal.acm.org

... Ta- ble 2 reports the **statistics** of the designs. ... simulations X values were constantly generated on **tri-state** buses, indicating **bus** con- tentions, which ... Cited by 37 - Web Search - BL Direct